ABSTRACT OF THE DISCLOSURE

The present invention includes a $6F^2$ DRAM array formed on a semiconductor substrate. The memory array includes a first memory cell. The first memory cell includes a first access transistor and a first data storage capacitor. A first load electrode of the first access transistor is coupled to the first data storage capacitor via a first storage node formed on the substrate. The memory array also includes a second memory cell. The second memory cell includes a second access transistor and a second data storage capacitor. A first load electrode of the second access transistor is coupled to the second data storage capacitor via a second storage node formed on the substrate. The first and second access transistors have a gate dielectric having a first thickness. The memory array further includes an isolation gate formed between the first and second storage nodes and configured to provide electrical isolation therebetween. The isolation gate has a gate dielectric having a second thickness that is greater than the first thickness. The isolation gate dielectric may extend above or below a surface of the substrate.